



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,730	08/21/2003	Shinsaku Sekido	60188-630	6195
7590	10/18/2006		EXAMINER	
Jack Q. Lever, Jr. McDERMOTT, WILL & EMERY 600 Thirteenth Street, N.W. Washington, DC 20005-3096			PIERRE LOUIS, ANDRE	
			ART UNIT	PAPER NUMBER
			2123	

DATE MAILED: 10/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/644,730	SEKIDO ET AL.
	Examiner Andre Pierre-Louis	Art Unit 2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 04 August 2006.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-11 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-11 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____.	6) <input type="checkbox"/> Other: _____.

DETAILED ACTION

1. The amendment filed on 08/04/2006 has been received and fully considered; claims 1-11 are presented for examination.

Response to Arguments

2. Applicant's arguments filed 08/04/2006 have been entered and fully considered.

2.1 In response to perfecting the priority document submitted on 08/04/2006, the examiner has withdrawn the previous rejection of the claims and a new rejection is set forth below.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." State Street, 149 F.3d at 1373, 47USPQ2d at 1601-02. The purpose of this requirement is to limit patent protection to inventions that possess a certain level of "real world" value, as opposed to subject matter that represents nothing more than an idea or concept, or is simply a starting point for future investigation or research (Brenner v. Manson, 383 U.S. 519, 528-36, 148 USPQ 689, 693-96); In re Ziegler, 992, F.2d 1197, 1200-03, 26 USPQ2d 1600, 1603-06 (Fed. Cir. 1993)). Accordingly, a complete disclosure should contain some indication of the practical application for the claimed invention, i.e., why the applicant believes the claimed invention is useful. However, the mere fact that the claim may satisfy the utility requirement of 35 U.S.C. 101 does not mean that a useful result is

achieved under the practical application requirement. The claimed invention as a whole must produce a "useful, concrete and tangible" result to have a practical application.

3.0 Claims 1-11 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims do not produce a useful, tangible, concrete result. **See MPEP 2106 [R2]**

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4.0 Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. (USPG_PUB No. 20030228714), in view of Yonezawa et al. (U.S. Patent No. 6,795,802).

4.1 In considering the independent claim 1, Smith et al. substantially teaches a circuit simulation method comprising the steps of (a) recognizing, from mask layout data for an integrated circuit, the shape of an electronic device to be analyzed which is provided in the integrated circuit, and obtaining data concerning the size of the electronic device to be analyzed (*fig.7, 15, and 16, also para 160-169, 215*); (b) determining the electrical characteristic of an electronic device for measurement, and measuring the size of each portion of the electronic device for measurement, as well as items each serving as an index of a stress applied to the electronic device to be analyzed (*fig.7(33-2), 15-16(36-14)*); (c) extracting, based on at least the size of each portion of the electronic device for measurement, parameters from data concerning the electrical characteristic of the electronic device for measurement which has been determined in the step (b) (*fig.7(31), 15-16*); and (d) utilizing a circuit simulator to select, from among the extracted parameters, a parameter suitable for each electronic device to be analyzed which is provided in the integrated circuit, and to perform circuit simulation in consideration of a stress applied to each electronic device to be analyzed (*fig.7,15-16, also para 106-110,119,183*). Smith et al. does not clearly teach applied stress to the device. Yonezawa et al. teaches applied stress and further teaches a stress calculation unit (*fig.5 (111b), col.7 line 43-col.10 line 65; also col.12 line 61-col.14 line 49*). It would have been obvious to one ordinary skilled in the art at the time of the applicant's invention to combine the stress calculation of Yonezawa et al. in the circuit simulation method of Smith et al. for the purpose of calculating and analyzing the stress

applied to the device. Yonezawa et al. further teaches the improvement of processing efficiency (*col. 12 lines 25-45*).

4.2 With regards to claim 2, the combined teachings of Smith et al and Yonezawa et al. substantially teach the step (b), at least an item serving as an index of a stress applied from an isolation insulating film to the electronic device to be analyzed is measured, and wherein in the step (d), the circuit simulation is performed in consideration of the stress applied from the isolation insulating film to the electronic device to be analyzed (see *Yonezawa et al. fig. 4-5, 12, col. 9 line 11-col. 10 line 51; also see Smith et al. 7, 15-16, and 25*).

4.3 As per claim 3, the combined teachings of Smith et al and Yonezawa et al. substantially teach in the step (c), a plurality of parameters are extracted for each of the equal-sized electronic devices to be analyzed, based on the items each serving as an index of a stress applied to the electronic device to be analyzed (see *Smith et al. fig. 7 (31), 15-16,25 (31); also Yonezawa et al. fig. 4-5, item 103*).

4.4 Regarding claim 4, the combined teachings of Smith et al and Yonezawa et al. substantially teach the step of inputting an additional model to the circuit simulator, the additional model being prepared based on measurement data that has been obtained in the step (b) and that serves as an index of a stress, and wherein in the step (d), a correction is made using the additional model when selecting a parameter suitable for each electronic device to be analyzed which is provided in the integrated circuit (see *Smith et al. fig. 7, 23-25, also para 154-160,183, 221; also Yonezawa et al. fig. 4-5*).

4.5 With regards to claim 5, the combined teachings of Smith et al and Yonezawa et al. substantially teach the step of preparing a reference table including pieces of information for associating each electronic device to be analyzed, which is provided in the integrated circuit, with the parameter that should be assigned to the electronic device to be analyzed, and the step of inputting the reference table to the circuit simulator, the reference table being prepared based on the items each serving as an index of a stress applied to the electronic device to be analyzed, and wherein in the step (d), the selection of the parameter suitable for each electronic device to be analyzed which is provided in the integrated circuit is automatically carried out using the reference table (see *Smith et al. fig.7, 11 15-17, (item 34-1 of fig.7), also para 155-166*); also *Yonezawa et al. fig.4-6*).

4.6 As per claim 6, the combined teachings of Smith et al and Yonezawa et al. substantially teach that the reference table is used to associate each electronic device to be analyzed, which is provided in the integrated circuit, with a plurality of weighted parameters (see *Smith et al. fig.7, 11 15-17, also para 155-166*); also *Yonezawa et al. fig.4-6*).

4.7 Regarding claim 7, the combined teachings of Smith et al and Yonezawa et al. substantially teach the electronic device to be analyzed and the electronic device for measurement are each formed by a MIS transistor or a bipolar transistor (see *Smith et al. fig.7, 11 15-17*), also para 155-166); also *Yonezawa et al. fig.4-6*).

4.8 With regards to claim 8, the combined teachings of Smith et al and Yonezawa et al. substantially teach wherein the electronic device to be analyzed and

the electronic device for measurement are each formed by a MIS transistor comprising a gate electrode, a gate insulating film, an active region and an isolation insulating film surrounding the active region, and wherein the items, each serving as an index of a stress applied to the electronic device to be analyzed, include at least one of the position of the gate electrode in the active region, the size of the active region, and the width of the isolation insulating film (see *Smith et al. fig.7, 11 15-17*, also para 155-166); also *Yonezawa et al. fig.4-6*).

4.9 As per claim 9, the combined teachings of Smith et al and Yonezawa et al. substantially teach wherein the items, each serving as an index of a stress applied to the electronic device to be analyzed, further include at least one of the depth of the active region, a method for forming the isolation insulating film, the depth of the isolation insulating film, a material for use in forming the isolation insulating film, the size of the gate insulating film, and a material for use in forming the gate insulating film (see *Smith et al. fig.7, 11 15-17*, also para 155-166); also *Yonezawa et al. fig.4-6*).

4.10 Regarding claim 10, the combined teachings of Smith et al and Yonezawa et al. substantially teach in the step (d), the circuit simulation is performed in consideration of a stress applied from the gate insulating film to the electronic device to be analyzed ((see *Smith et al. fig.7, 11 15-17*, also para 155-166); also *Yonezawa et al. fig.4-6*).

4.11 As per claim 11, the combined teachings of Smith et al and Yonezawa et al. substantially teach in the step (b), at least an item that serves as an index of a stress applied from an interlayer dielectric film to the electronic device to be analyzed is

measured, and wherein in the step (d), the circuit simulation is performed in consideration of the stress applied from the interlayer dielectric film to the electronic device to be analyzed (see *Yonezawa et al. fig. 4-5, 12, col.9 line 11-col.10 line 51; also see Smith et al. 7, 15-16, and 25*).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5.1 Krabbenborg et al. (IEEE 1996) teaches a Layout to Circuit Extraction for Three-Dimension Thermal-Electrical Circuit Simulation of Device Structures, Pgs.765-774.

5.2 Taravade et al. (USPG_PUB No. 2004/0040000) teaches a device parameter and gate performance simulation based on wafer image prediction.

5.3 Venugopal et al. (USPG_PUB No. 2002/0152447) teaches an integrated circuit design error detector for electrostatic discharge and latch-up applications.

5.4 Toda (U.S. Patent No. 6,144,931) teaches a wafer expansion and contraction simulation method.

5.5 White et al. (USPG_PUB No. 203/0237064) teaches a characterization and verification for integrate circuits designs.

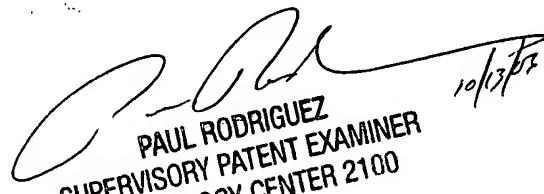
6. Claims 1-11 are rejected and **THIS ACTION IS Non-FINAL**. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre Pierre-Louis whose telephone number is 571-272-8636. The examiner can normally be reached on Mon-Fri, 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

October 11, 2006

APL



10/13/06

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100